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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/676,445 | 09/30/2003 | Amit Singh | X-1494 US | 7027 |

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| EXAMINER | |
|---|---|
| LIN, SUN J | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2825 | |

DATE MAILED: 09/19/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/676,445 | SINGH ET AL. | |
| | Examiner | Art Unit | |
| | Sun J. Lin | 2825 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *30 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *21-30* is/are allowed.

6)☒ Claim(s) *1,7-10,12 and 17-20* is/are rejected.

7)☒ Claim(s) *2-6,11 and 13-16* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09/30/2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No: _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *9/30/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## *DETAILED ACTION*

1. This office action is in response to application 10/676,445 filed on 09/30/2003. Claims 1 – 30 remain pending in the application.

### *Drawing Objections*

2. Drawings are objected to because of following informalities:

FIG. 1A should be labeled as a **—(PRIOR ART)—**.
FIG. 1B should be labeled as a **—(PRIOR ART)—**.
FIG. 2 should be labeled as a **—(PRIOR ART)—**.

Appropriate corrections are required.

### *Claim Objections*

3. Claims listed below are objected to because of the following informalities:

Claim 1, line 3, change "the steps of:" to **—the following steps:—** or **—steps of:—**.
Claim 1, line 10, change "the arrival times and the propagation delays" to **—arrival times associated with the plurality of input signals and propagation delays associated with the plurality of input ports of the component—**.
Claim 3, line 3, change "an identified topological level" to **—one of said identified topological levels—**.
Claim 4, line 2 – 3, change "each identified topological level" to **—each of said identified topological levels—**.
Claim 5, line 1, before "topological" insert **—identified—**.
Claim 7, line 2, change "the step" to **—a step—**.
Claim 8, line 2, change "an earliest" to **—the earliest—**.
Claim 8, line 3, change "a longest" to **—the longest—**.
Claim 8, line 4, change "a latest" to **—the latest—**.
Claim 8, line 5 – 6, change "a shortest" to **—the shortest—**.
Claim 9, line 6, before "input signals" insert **—said sorted—**.
Claim 9, line 7, before "input ports" insert **—said sorted—**.
Claim 9, line 7, delete **—of the component—**.
Claim 10, line 2, change "an earliest" to **—the earliest—**.

Claim 10, line 3, change "a longest" to —**the longest**—.
Claim 10, line 4, change "a latest" to —**the latest**—.
Claim 10, line 5, change "a shortest" to —**the shortest**—.
Claim 12, line 4, before "propagation" delete to —**the**—.
Claim 12, line 7, change "times" to —**time**—.
Claim 15, line 1, change "claim 13" to —**claim 14**—.
Claim 15, line 2, after "each" insert —**of**—.
Claim 15, line 2, change "level" to —**levels**—.
Claim 18, line 2, change "an earliest" to —**the earliest**—.
Claim 18, line 3, change "a longest" to —**the longest**—.
Claim 18, line 4, change "a latest" to —**the latest**—.
Claim 18, line 5, change "a shortest" to —**the shortest**—.
Claim 20, change "an earliest" to —**the earliest**—.
Claim 20, line 3, change "a longest" to —**the longest**—.
Claim 20, line 4, change "a latest" to —**the latest**—.
Claim 20, line 5, change "a shortest" to —**the shortest**—.
Claim 21, line 3, change "the steps of:" to —**the following steps:**— or —**steps of:**—.
Claim 21, line 7, before "propagation" delete to —**the**—.
Claim 21, line 9, change "lookup" to —**look up**—.
Claim 21, line 10, change "times" to —**time**—.
Claim 22, line 1, change "machine readable storage" to —**computer program**—.
Claim 22, line 2, change "the step" to —**a step**—.
Claim 23, line 1, change "machine readable storage" to —**computer program**—.
Claim 23, line 2, change "the step" to —**a step**—.
Claim 24, line 1, change "machine readable storage" to —**computer program**—.
Claim 24, line 2, change "the step" to —**a step**—.
Claim 25, line 1, change "machine readable storage" to —**computer program**—.
Claim 25, line 2, before "topological" insert —**identified**—.
Claim 26, line 1, change "machine readable storage" to —**computer program**—.
Claim 26, line 2, change "the step" to —**a step**—.
Claim 27, line 1, change "machine readable storage " to —**computer program**—.
Claim 27, line 1, before "said" insert —**wherein**—.
Claim 27, line 2, change "the step" to —**a step**—.
Claim 27, line 3, change "lookup" to —**look up**—.

Claim 28, line 1, change "machine readable storage" to —**computer program**—.
Claim 28, line 3, change "lookup" to —**look up**—.
Claim 28, line 5, change "lookup" to —**look up**—.
Claim 29, line 1, change "machine readable storage" to —**computer program**—.
Claim 29, line 1, before "said" insert —**wherein**—.
Claim 30, line 1, change "machine readable storage" to —**computer program**—.
Claim 30, line 2, change "an earliest" to —**the earliest**—.
Claim 30, line 3, change "lookup" to —**look up**—.
Claim 30, line 3, change "a longest" to —**the longest**—.
Claim 30, line 4, change "a latest" to —**the latest**—.
Claim 30, line 5, change "a shortest" to —**the shortest**—.

Appropriate corrections are required.

***Claim Rejections - 35 USC § 103***

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

(1). Determining the scope and contents of the prior art.
(2). Ascertaining the differences between the prior art and the claims at issue.
(3). Resolving the level of ordinary skill in the pertinent art.
(4). Considering objective evidence present in the application indicating obviousness or nonobviousness.

5. Claims 1, 7 – 10, 12 and 17 – 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over IBM technical paper title "*Bus Deskewing Method using a Self-Adjusting Variable Delay Element*" published in IBM Technical Disclosure Bulletin (called IBM_TDB hereinafter) in view of industrial common practice.

6. As to Claim 1, IBM_TDB discloses the following subject matter:

- Bus deskewing method for compensating *arrival time differences* among *input signals* of by *adjusting propagation delay* of each signal path in data bus of a circuit design – [title; disclosure text];
- Estimating (i.e., determining) an arrival time for each input signal – [disclosure text];
- Identifying propagation delay along (signal path) associated with each input signal – [disclosure text];
- Variable propagation delays are applied to input signals with different arrival times in order to allow the input signals to reach outputs approximately at *the same time* – [disclosure text].

IBM_TDB does not teach ordering input signals according arrival times and the propagation delays. But, it is an industrial common practice that the orders of input signals feeding to input terminals of a data circuit design can be rearranged according to arrival times associated with the input signals and propagation delays associated with propagation paths in order to allow the input signals to reach outputs approximately the same time without modifying the hardware of the data circuit design.

Therefore, it would have been obvious at the time the invention was made to a person having ordinary skill in the art to have applied industrial common practice in rearranging the orders of the input signals feeding to input terminals of a data circuit design according to arrival times associated with the input signals and propagation delays associated with propagation paths in order to allow the input signals to reach outputs approximately the same time without modifying the hardware of the data circuit design.

For reference purposes, the explanations given above in response to Claim 1 are called **[Response A]** hereinafter.

7. As to Claim 12, reasons are included in **[Response A]** given above.

8. As to Claims 7 – 10, the reasons are included in **[Response A]** given above due to the fact that the variable propagation delays are applied to input signals with different arrival times in order to allow the input signals to reach outputs approximately at the same time. It is well

known in the art that the ordering step comprises sorting input signals, sorting input ports and matching input signals

For reference purposes, the explanations given above in response to Claims 7 – 10 are called **[Response B]** hereinafter.

9. As to Claims 17 – 20, reasons are included in **[Response B]** given above.

***Allowable Subject Matter***

10. Claims 21 – 30 are allowed. Claims 2 – 6, 11 and 13 – 16 are objected to as being dependent upon a rejected base claim, but they would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Those claims are allowed is because that the prior art does not teach or fairly suggest the following subject matter:

- A method of placing a circuit design comprising a component having input signals with asymmetric delays, the method comprises a step of *first identifying topological levels of the circuit design* in combination with other limitations as recited in **Claim 2**;
- A method of placing a circuit design comprising a component having input signals with asymmetric delays wherein the component is a look up table in combination with other limitations as recited in **Claim 11**;
- A system for placing a circuit design comprising *means for determining an arrival time for each input signal to a component within a circuit design representation* wherein the component is a look up table in combination with other limitations as recited in **Claim 13**;
- A machine readable storage having stored thereon a computer program, having a plurality of code sections, executable by a machine for causing the machine to perform a step of *ordering input signals of a look up table (LUT) according to arrival time of each input signal to the LUT and propagation delay of each pin of the LUT* in combination with other limitations as recited in independent **Claim 21**.

***Conclusion***

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sun J Lin whose telephone number is (571) 272 - 1899. The examiner can normally be reached on Monday-Friday 9:30AM - 6:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S Smith can be reached on (571) 272 - 1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Sun J. Lin
Patent Examiner
Art Unit 2825
September 17, 2005